United Electronic Industries

The High-Performance Alternative

DNx-AI-201

—

User Manual

Sequential Sampling, 16-bit, 24-channel Analog Input board for the PowerDNA Cube and RACK series chassis

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PN Man-DNx-AI-201

CE

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Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-201 board.

The AI-201 is a 24-channel single ended, 12-channel differential analog input board for the PowerDNA I/O Cube (DNA-AI-201), the PowerDNR HalfRACK & RACKtangle (DNR-AI-201), and the FLATRACK chassis (DNF-AI-201).

The following sections are provided in this chapter:

- Organization of this Manual (Section 1.1)
- AI-201 Board Overview (Section 1.2)
- Features (Section 1.3)
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- Device Architecture (Section 1.5)
- Indicators (Section 1.6)
- Connectors and Wiring (pinout) (Section 1.7)
- Board Capabilities (Section 1.8)

1.1 Organization of this Manual

This AI-201 User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-AI-201 Analog Input Board features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  This chapter is an overview of low-level API commands for configuring and using the AI-201 series board.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-201 board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

NOTE: A glossary of terms used with the PowerDNA Cube/RACK and I/O boards can be viewed or downloaded from www.ueidaq.com.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Bold typeface will also represent field or button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbatim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 AI-201 Board Overview

The DNx-AI-201 is a 24-channel single ended, 12-channel differential A/D board. The DNA-boards are compatible with all of the Cube series chassis while the DNR-boards are used in the RACKtangle® I/O series chassis and DNF-boards are used in the FLATRACK chassis. All versions provide identical electrical specifications and performance including 16-bit resolution with a maximum input range of ±15 V. The board is fully isolated from the PowerDNA chassis and is an ideal A/D board for a wide variety of high speed, high resolution data acquisition (DAQ) and control applications.

1.3 Features

The AI-201 board has the following features:

- 24 single-ended/12 differential inputs
- ±15V input range
- Gains of 1/2/5/10, per-channel selectable, maximum speed is 100 kS/sec on multiple channels (aggregate)
- Completely configurable per-channel settling time delay with better than 1 µS resolution
- 16-bit resolution, no missing codes
- ± 40 V overvoltage, 2 kV ESD protection on all input pins
- All analog I/O is fully opto-isolated from the rest of the system
- Auto-calibration (software initiated)
- Precision, digitally calibrated to 0.001%, 3 ppm/°C on-board reference
- 1k samples input FIFO with 32-bit per-sample timestamp
- Interrupt request on any position in the input or channel list FIFO
- On-board EEPROM to store configuration and calibration data
- Input ground to system ground isolation: $350V_{rms}$
- Power consumption ~ 1.6 / 2.2 W
- Weight of 120 g or 4.24 oz for DNA-AI-217; 630 g or 22.2 oz with PPC5
- UEI Framework Software API may be used with all popular Windows programming languages and most real time operating systems such as RT Linux, RTX, or QNX and graphical applications such as LabVIEW, MATLAB, and any application supporting ActiveX or OPC.

1.4 Specification

The technical specification for the DNx-AI-201-100 board is listed in **Table 1-1**.

Table 1-1 . DNx-AI-201-100 Technical Specifications

Resolution	16 bits
Number of Channels: Single-Ended Differential	 24 12
Maximum Sampling Rate	100 kS/s, aggregate
Onboard FIFO Size	512 samples
Input Range	±15V
Programmable Gains	1, 2, 5, 10 (by channel)
Input Impedance	10 MΩ
Input Bias Current	±15 nA
Input Overvoltage	±40V, 2000V ESD powered or unpowered
A/D Conversion Time	2 µs
A/D Settling Time	10µs @ G=1; 15µs @ G=2; 25µs @ G=5; 50µs @ G=10
Nonlinearity	1 LSB
System Noise	1.2 LSB
Isolation	350V_{rms}
Effective Number of Bits	14.8
Total Harmonic Distortion+Noise+Noise	91 dB
Channel Crosstalk	85 dB @ 1 kS/s
Power Consumption	2.0W
Physical Dimensions	3.875 x 3.875”(98 x 98 mm)
Operating Temp. (tested)	-40°C to +85°C
Operating Humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations

1.5 Device Architecture

Figure 1-1 is a block diagram of the architecture of the AI-201 board.

The DNx-AI-201 board is physically divided into isolated and non-isolated sections. The non-isolated section is powered from DC/DC converters located on the CPU board. These converters provide 5 V and 3.3 / 2.5 V to power all non-isolated electronics.

The isolating DC/DC that produces 5 V powers the isolated side of the board. Two high-frequency boosters generate +18 V, -18 V rails that are also available on the connector (15 mA maximum each).
On the AI-201-801 this is +2.5 V, -18 V.

The DNx-AI-201 employs a single successive-approximation converter with no pipeline delay.

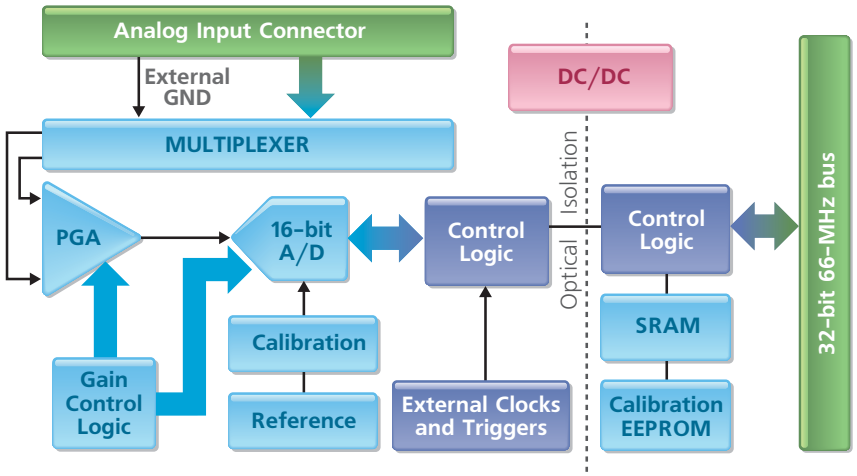


Figure 1-1 Architecture Block Diagram of the AI-201 Board

1.6 Indicators

The DNx-AI-201 indicators are described in **Table 1-2** and illustrated in **Figure 1-2**.

Table 1-2 AI-201 Indicators

LED Name	Description
RDY	Indicates board is powered up and operational
STS	Indicates which mode the board is running in: • **OFF**: Configuration mode, (e.g., configuring channels, running in point-by-point mode) • **ON**: Operation mode, (e.g., running in VMap or ACB mode)

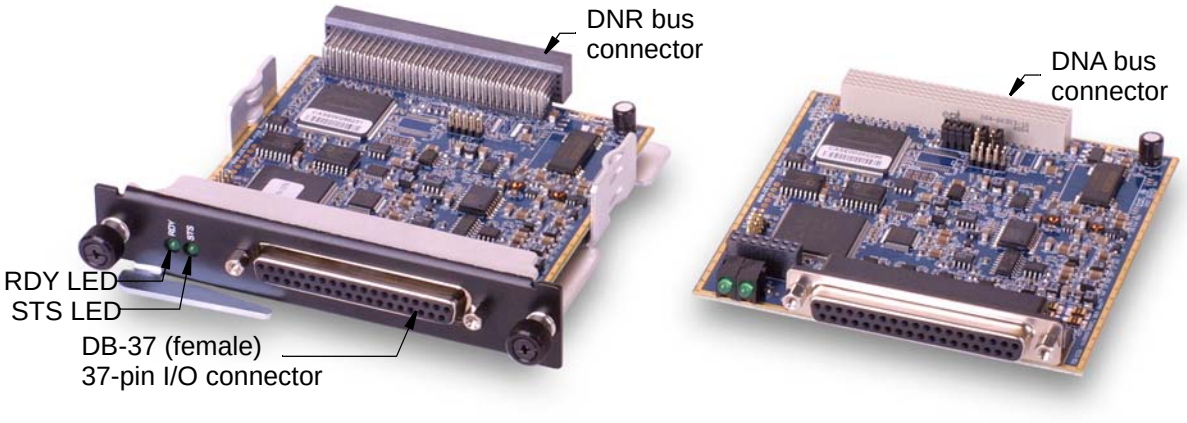


Figure 1-2 The DNx-AI-201 Analog Input Boards

1.7 Connectors and Wiring (pinout)

Figure 1-3 below shows the pinout of the AI-201-100 and AI-201-801.

The AI-201 uses a B-size 37-pin D-sub connector for all I/O connections.

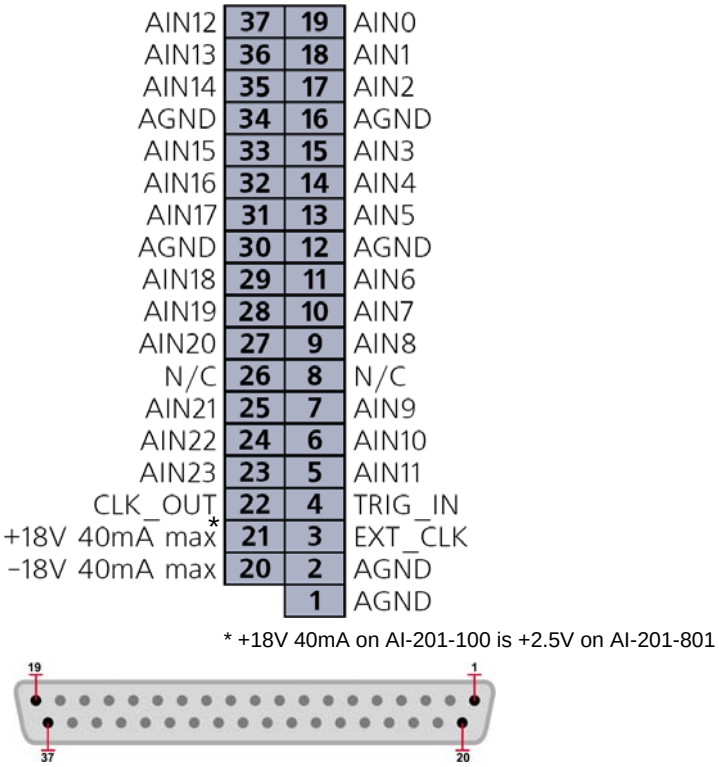


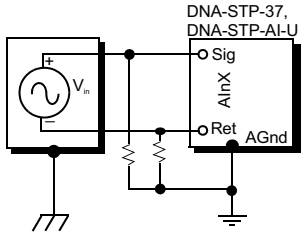
Figure 1-3 Pinout of the DNx-AI-201

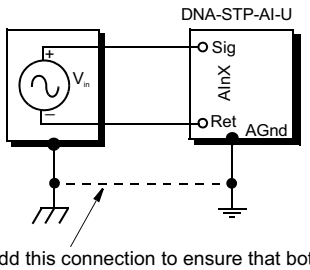
The following signals are located at the connector:

- ***AIn0 – AIn23*** input channels. If a channel is set to operate as single-ended, its voltage is measured between the selected channel line and the analog ground (*AGND*) line. If Channel X is used as a differential measurement, its inputs are connected between Channel *AIn(X)* and *AIn(X+12).* For example, in differential mode, channel *AIn0* pairs with *AIn12*, *AIn1* with *AIn13*, etc.
- ***AGND*** analog ground of the board, isolated from system ground.
- ***CLKOUT*** output used as an external channel list clock that can be used to synchronize multiple PowerDNA chassis.
- ***TRIGIN*** input that provides an external trigger signal to the board.
- ***EXTCLK*** input that provides an external clock to the board logic.
- ***+18V, -18V*** lines on the AI-201-100 provide isolated voltage generated on the board to power external sensors. As maximum current is limited to 15 mA each, we suggest using large current-limiting resistors when using this source to power strain gages or RTDs.
  On the AI-201-801 the reference is +2.5 V, -18 V instead.

1.7.1 Analog Input Ground Connections

To avoid errors caused by common mode voltages on analog inputs, follow the recommended grounding guidelines in **Figure 1-4** below.

<table>
<tr><th rowspan="2">Input Configuration</th><th colspan="2">Type of Input</th></tr>
<tr><th>Floating</th><th>Grounded</th></tr>
<tr><td></td><td>Typical Signal Sources:
Thermocouples
DC Voltage Sources
Instruments or sensors with isolated outputs</td><td>Typical Signal Sources:
Instruments or sensors with non-isolated outputs</td></tr>
<tr><td>Differential</td><td> 

Two resistors (10k <R< 100k) provide return paths to ground for bias currents.</td><td> 

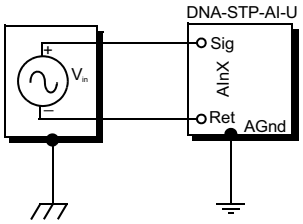
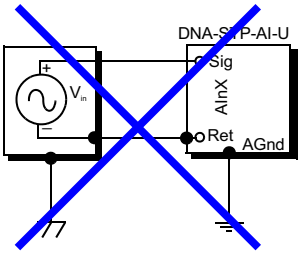
Add this connection to ensure that both grounds are at the same potential.</td></tr>
<tr><td>Single-Ended, Ground Referenced</td><td> 
</td><td>NOT RECOMMENDED
 
</td></tr>
</table>

Figure 1-4 Recommended Ground Connections for Analog Inputs

Because all analog input channels in AI-201/202/207/208/225 boards are isolated as a group, you can connect board AGND to the ground of the signal source and eliminate the resistors shown in **Figure 1-4** for floating differential input signals.

1.8 Board Capabilities

The AI-201 board is capable of acquiring analog input voltage in the ±15 V range with programmable gains of 1, 2, 5, 10.

A board is capable of generating its own conversion clocks and trigger and deriving them from either local external lines from its connector or from the SYNCx bus.

You can connect a signal source to the board using either differential or single-ended wiring. Because of this, the ground plane is isolated from the system ground; single ended and pseudo-differential wiring use effectively the same wiring.

Table 1-3 . Gains

Card	Gain	Range	Settling Time to 16-bit Resolution	Noise, LSB	Resolution, Noise Limited
DNA-AI-201-100 & DNA-AI-201-801	1	±15V	10µs	1.04	457 µV
	2	±7.5V	15µs	1.28	228 µV
	5	±3V	25µs	2.20	91 µV
	10	±1.5V	50µs	3.11	45 µV

1.8.1 Single-Ended and Pseudo-Differential

An AI-201 board operating in single-ended mode digitizes across as many as 24 channels. For single-ended inputs, you connect one wire from each signal source to the High input of the input amplifier to the data-acquisition system. All signals share a common return path connected to analog ground (AGND). You should connect this common return path both to a ground near the signal source and also to the ground on the PC, which forces it to be the same level as the signal ground. This ground signal, however, is typically referenced to a remote source and because it is separated from the system ground, it can float at a different level. The maximum potential difference between common ground and PC ground should never exceed 350V. Because the AGND line in a pseudo-differential setup is not connected to the computer ground, however, it is not subject to the associated digital noise within the system.

1.8.2 Differential

An AI-201 board operating in differential mode digitizes as many as 12 channels. Each channel uses two lines on the input amplifier of the data-acquisition system: you connect one lead from the signal source to the channel's High input (the positive input of the amp) and connect the other signal lead to the channel's Low input (the amp's negative input). Each signal floats at its own level without any reference to ground or other inputs.

When working with a DNx-AI-201 board in differential mode, AIn0 and AIn12 form the High and Low inputs of differential-input Ch 0; next, for differential-input Ch 1, use AIn1 and AIn13; follow this pattern for all twelve differential-input pairs.

Two high-impedance amplifiers monitor the voltage between the inputs and the PC ground. A third amplifier measures the difference between the Positive and Negative inputs, eliminating any voltage common to both wires. This method eliminates problems that can arise with a single-ended system because this configuration attenuates noise common to both channel inputs (common-mode noise). Thus, it's wise to use twisted-pair cable to bring signals to the data-acquisition board because that setup ensures that any noise generated along the wiring path is the same for each line, and the amplifier subtracts this noise.

Although using differential inputs cuts the number of channels you can read with a given board in half compared to single-ended or pseudo-differential setups, there are several cases where you are well advised to use differential inputs, such as:

- When signal leads are over a few meters in length.The instrumentation amp can eliminate the effect of noise pickup from signal leads and eliminate the possibility of ground differentials.
- When signals are less than approximately 100 mV. Such low-level signals can be easily overwhelmed by noise and ground differentials that only the differential mode can remove.
- When the signals are from high-impedance sensors such as strain gauges. Their high impedances can lead to higher common-mode voltages, which differential inputs are able to remove.

1.8.3 Data Presentation

The AI-201 board is equipped with a single A/D converter, and can return a 16-bit 2s complement data word.

16-bit data is represented as follows:

Bit	Name	Description	Reset State
15	**SIGN**	Sign. Signal levels below 0V correspond with negative values (sign bit is set).	0
14-0	**ADCDATA**	Upper 15 bits of data, twos-complemented	**<pos>**

<pos> represents a position in the output buffer. Upon reset, every entry in the output buffer is filled with its relative position number. As an initializing step, you should read the buffer and discard the data before proceeding with normal data collection.

If you start receiving consecutive data from the board, (i.e., 0, 1, 2, etc.), it means that either the board is not initialized properly or it is damaged.

To convert data into floating point, use the following formula:

```
Volts = (Raw ^ 0x8000) * (30V/2^16) – 15V
```

Note this formula is for gains of 1.

Chapter 2 Programming with the High Level API

This chapter provides the following information about using the UeiDaq high-level Framework API to program the DNx-AI-201:

- About the High-Level Framework (Section 2.1)
- Creating a Session (Section 2.2)
- Configuring the Resource String (Section 2.3)
- Configuring for Input (Section 2.4)
- Configuring the Timing (Section 2.5)
- Reading Data (Section 2.6)
- Cleaning-up the Session (Section 2.7)

2.1 About the High-Level Framework

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments, such as Visual C++, Visual Basic, or LabVIEW.

UeiDaq Framework is bundled with examples for supported programming languages. Examples are located under the UEI programs group in:

- *Start » Programs » UEI » Framework » Examples*

The following sections focus on the C++ API, but the concept is the same no matter which programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.2 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input
                    CUeiSession aiSession;
```

2.3 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

2.4 Configuring for Input

The AI-201 can be configured for voltage measurement input. To program the analog input circuitry, configure the channel list using the session's object method "CreateAIChannel".

The gain applied on each channel is specified by using low and high input limits.

For example, the DNA-AI-201-100 available gains are 1, 2, 5, 10 and the maximum input range is [-15V, 15V].

To select the gain of 10, you need to specify input limits of [-1.5V, 1.5V]:

```
// Configure channels 0,1 to use gain of 10 in differential mode

aiSession.CreateAIChannel("pdna://192.168.100.2/Dev0/Ai0,1",
                          -1.5,
                           1.5,
                          UeiAIChannelInputModeDifferential);
```

Be mindful of your gain setting. Note that when reading any of the channels in point-by-point mode, the hardware actively keeps the data just below the gain limit. When the gain is set too high, the output will appear as an inverted approximate of the actual signal, scaled down under the gain limit. Try a lower gain value, or begin with one.

2.4.1 RTD Measurement

Resistance-Temperature-Detector (RTD) measurements are configured using the Session object method "CreateRTDChannel".

RTD sensors are resistive sensors whose resistance varies with temperature. Knowing the resistance of an RTD, we can calculate the temperature using the "Callendar Van-Dusen" equations.

RTD sensors are specified using the "alpha" (a) constant. It is also known as the temperature coefficient of resistance, which defines the resistance change factor per degree of temperature change. The RTD type is used to select the proper coefficients A, B and C for the Callendar Van-Dusen equation, which is used to convert resistance measurements to temperature.

To measure the RTD resistance, we need to know the amount of current flowing through it. We can then calculate the resistance by dividing the measured voltage by the known excitation current.

To measure the excitation current, we measure the voltage from a high precision reference resistor whose resistance is known.

The reference resistor is built-into the terminal block if you are using a DNA-STP-AI-U, but you can provide your own external reference resistor, if you prefer.

In addition, you must configure the RTD type and its nominal resistance at 0° Celsius, as shown in the example that follows.

```
// Add 4 channels (0 to 3) to the channel list and configure
// them to measure a temperature between 0.0 and 200.0 deg. C.
// The RTD sensor is connected to the DAQ device using
// two wires, the excitation voltage is 5V, and the reference
// resistor is the 20kOhms resistor built-into the DNA-STP-AI-U.
// The RTD alpha coefficient is 0.00385, the nominal resistance at 0° C
// is 100 Ohms, and the measured temperature will be returned in °C

aiSession.CreateRTDChannel("pdna://192.168.100.2/dev0/Ai0:3",
                           0, 1000.0,
                           UeiTwoWires,
                           5.0,
                           UeiRefResistorBuiltIn,
                           20000.0,
                           UeiRTDType3850,
                           100.0,
                           UeiTemperatureScaleCelsius,
                           UeiAIChannelInputModeDifferential);
```

2.5 Configuring the Timing

You can configure the AI-201 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode.

In simple mode, the delay between samples is determined by software on the host computer. In DMAP mode, the delay between samples is determined by the AI-201 on-board clock and data is transferred one scan at a time between PowerDNA and the host PC. In buffered mode, the delay between samples is determined by the AI-201 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the "UeiDaq Framework User's Manual" to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)

aiSession.ConfigureTimingForSimpleIO();
```

2.6 Reading Data

Reading data is done using *reader* object(s). The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session's stream

CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());

// the buffer must be big enough to contain one value per channel

double data[2];

// read one scan, where the buffer will contain one value per channel

aiReader.ReadSingleScan(data);
```

2.7 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

Chapter 3 Programming with the Low-level API

This chapter provides the following information about programming the AI-201 using the low-level API:

- About the Low-level API (Section 3.1)
- Low-level Functions (Section 3.2)
- Low-level Programming Techniques (Section 3.3)
- Configuration Settings (Section 3.4)
- Board-specific Commands & Parameters (Section 3.5)

3.1 About the Low-level API

The low-level API provides direct access to the DAQBIOS protocol structure and registers in C. The low-level API is intended for speed-optimization, when programming unconventional functionality, or when programming under Linux or real-time operating systems.

When programming in Windows OS, however, we recommend that you use the UeiDaq high-level Framework API (see **Chapter 2**). The Framework extends the low-level API with additional functionality that makes programming easier, faster, and less error-prone.

For additional information regarding low-level programming, refer to the "PowerDNA API Reference Manual" located in the following directory:

- On Linux systems:
  <PowerDNA-x.y.z>/docs
- On Windows systems:
  Start » All Programs » UEI » PowerDNA » Documentation

3.2 Low-level Functions

Table 3-1 provides a summary of AI-201-specific functions. All low-level functions are described in detail in the PowerDNA API Reference Manual.

Table 3-1 Summary of Low-level API Functions for DNx-AI-201

Function	Description
`DqAdv201Read`	This function works using underlying DqReadAIChannel() but converts data using internal knowledge of input range and gain of every channel.

3.3 Low-level Programming Techniques

Application developers are encouraged to explore the existing source code examples when first programming the AI-201. Sample code provided with the installation is self-documented and serves as a good starting point.

Code examples are located in the following directories:

- For Linux: <PowerDNA-x.y.z>/src/DAQLib_Samples
- For Windows: *Start » All Programs » UEI » PowerDNA » Examples*

Sample code is provided for the data acquisition mode protocols that the AI-201 supports: point-to-point, Advanced Circular Buffer (ACB), Data Mapped I/O (DMAP), and Variable-data-size Mapped (VMAP).

Note that sample code for a specific data acquisition mode will have the data mode acronym and the board name embedded in the example name, except for the point-to-point mode example, which is called *Sample201*.

Data acquisition modes are described in detail in the *PowerDNx Protocol Manual,* and API that implement data acquisition modes are described in the *PowerDNA API Reference Manual*.

3.4 Configuration Settings

Configuration settings are passed to the `DqAcbInitOps()` function when the AI-201 is programmed in advanced circular buffer (ACB) mode.

The following configuration bits are set in the AI-201 ACB example:

```
// unit configuration word
#define CFG201          (DQ_LN_ENABLED \
                        |DQ_LN_ACTIVE \
                        |DQ_LN_GETRAW \
                        |DQ_LN_IRQEN \
                        |DQ_LN_CLCKSRC0 \
                        |DQ_LN_STREAMING \
                        |DQ_AI201_MODEFIFO)
```

- `DQ_LN_ENABLE` enables all operations with the board.
- `DQ_LN_CLCKSRC0` selects the internal channel list clock (CL) source as a timebase. AI-201 supports CL clock only, which means the time between consecutive channel readings is calculated by the rule of maximizing setup time per channel. To use an external clock source, such as the SYNCx line from a chassis-wide synchronized clock, set `DQ_LN_CLCKSRC1`.

An overview of the configuration bits for the AI-201 is described on the next page. A detailed description of configuration bits is listed in the *PowerDNA API Reference Manual*; however, not all configuration bits listed in *PowerDNA API Reference Manual* apply to AI-201 boards.

```
// Configuration bits

   #define DQ_FIFO_MODEFIFO (2L << 16)  // continuous
                                        // acquisition with FIFO
   #define DQ_LN_MAPPED     (1L<<15)    // For WRRD (DMAP) devices
   #define DQ_LN_STREAMING  (1L<<14)    // For RDFIFO devices -
                                        // stream the FIFO
                                        // data automatically
                                        // For WRFIFO - do NOT
                                        // send reply to
                                        // WRFIFO unless needed
   #define DQ_LN_IRQEN      (1L<<10)    // enable layer irqs
   #define DQ_LN_PTRIGEDGE1 (1L<<9)     // stop trigger edge MSB
   #define DQ_LN_PTRIGEDGE0 (1L<<8)     // stop trigger edge:
                                        // 00 - software,
                                        // 01 - rising,
                                        // 02 - falling
   #define DQ_LN_STRIGEDGE1 (1L<<7)     // start
                                        // trigger edge is MSB
   #define DQ_LN_STRIGEDGE0 (1L<<6)     // start trigger edge:
                                        // 00 - software,
                                        // 01- rising,
                                        // 02 - falling
   #define DQ_LN_CVCKSRC1   (1L<<5)     // CV clock source MSB
   #define DQ_LN_CVCKSRC0   (1L<<4)     // CV clock source is
                                        // 01 - SW, 10 - HW,
                                        // 11 - EXT
   #define DQ_LN_CLCKSRC1   (1L<<3)     // CL clock source MSB
   #define DQ_LN_CLCKSRC0   (1L<<2)     // CL clock source is
                                        // 01 - SW, 10 - HW,
                                        // 11 - EXT
   #define DQ_LN_ACTIVE     (1L<<1)     // "STS" LED status
   #define DQ_LN_ENABLED    (1L<<0)     // enable operations
```

3.5 Board-specific Commands & Parameters

The board-specific function for the AI-201, `DqAdv201Read(),` reads analog input data in point-to-point mode.

When this function is called for the first time, the firmware stops any ongoing operation on the device specified and reprograms it accordingly, with the channel list supplied. This function uses the preprogrammed CL update frequency of 10 Hz. You can reprogram the update frequency by calling the `DqCmdSetClk()` command after the first call to `DqAdv201Read()`.

If you specify a short timeout delay, this function can time out when called for the first time because it is executed as a pending command and board programming takes up to 10 ms.

Once this function is called, the board continuously acquires data, and the latest acquired data is returned every subsequent function call.

3.5.1 Channel List Settings

The `DqAdv201Read()` API is passed a channel list parameter for programming the order of the channels in the channel list and for programming the gain setting.

The channel list parameter is built by bitwise ORing the `#define` value representing the gain (**Table 3-2**) with the channel number. Refer to sample code for constructs and for examples of the `DQ_LNCL_CHANGAIN` and `DQ_LNCL_GAIN` macro utilities.

Table 3-2. AI-201-100 Gains

Board Type	Range	Gain	Gain #define Setting
AI-201-100	±15V	1	`DQ_AI201_GAIN_1_100`
	±7.5V	2	`DQ_AI201_GAIN_2_100`
	±3V	5	`DQ_AI201_GAIN_5_100`
	±1.5V	10	`DQ_AI201_GAIN_10_100`

Appendix A

A.1 Accessories

The following cables and STP boards are available for the AI-201 layer.

DNA-CBL-37

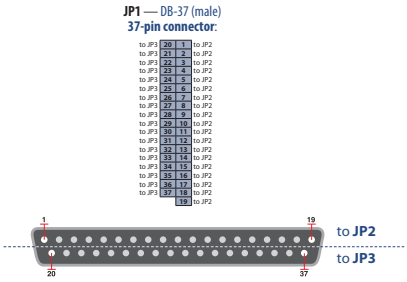
This is a 37-conductor flat ribbon cable with 37-pin male D-sub connectors on both ends. The length is 3ft and the weight is 3.4 ounces or 98 grams.

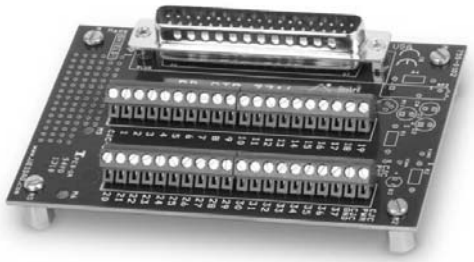
DNA-CBL-37S

This is a 37-conductor round shielded cable with 37-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 3 ft (90 cm) long, weight of 10 ounces or 282 grams; also available in 10ft and 20ft lengths.

DNA-STP-37

The DNA-STP-37 provides easy screw terminal connections for all DNA and DNR series I/O boards which utilize the 37-pin connector scheme. The DNA-STP-37 is connected to the I/O board via either DNA-CBL-37 or DNA-CBL-37S series cables. The dimensions of the STP-37 board are 4.2w x 2.8d x1.0h inch or 10.6 x 7.1 x 7.6 cm (with standoffs). The weight of the STP-37 board is 2.4 ounces or 69 grams.





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